MSR PROJECTS

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1.	First experimental demonstration of a scalable linear majority gate based on spin waves	Ieee -2018
2.	Design of Majority Logic Based Comparator	Ieee -2018
3.	Novel Cascadable Magnetic Majority Gates for Implementing Comprehensive Logic Functions	Ieee -2018
4.	Comparator Design using CTL and Outputwired based Majority Gate	Ieee -2018
5.	Design of Generalized Pipeline Cellular Array in Quantum-Dot Cellular Automata	Ieee -2018
6.	Size Optimization of MIGs with an Application to QCA and STMG Technologies	Ieee -2018
7.	Spin-based majority gates for logic applications	Ieee -2018
8.	Finite Hyperplane Codes: Minimum Distance and Majority-Logic Decoding	Ieee -2018
9.	Adapting Computer Arithmetic Structures to Sustainable Supercomputing in Low-Power, Majority-Logic Nanotechnologies	Ieee -2018
10.	A Novel Design of Quantum-Dots Cellular Automata Comparator Using Five-Input Majority Gate	Ieee -2018
11.	Modified majority logic decoding of Reed–Muller codes using factor graphs	Ieee -2018
12.	Characteristics of signal propagation in multiferroic majority logic gates subjected to thermal noise	Ieee -2018
13.	Bit error probability analysis for majority logic decoding of CSOC codes over fading channels	Ieee -2018
14.	Majority Voting-Based Reduced Precision Redundancy Adders	Ieee -2018
15.	On the Decoding Radius Realized by Low-Complexity Decoded Non-Binary Irregular LDPC Codes	Ieee -2018

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16.	Design of 2's Complement of 4-Bit Binary Numbers Using Quantum Dot Cellular Automata	Ieee -2018
17.	Majority Logic: Prime Implicants and n-Input Majority Term Equivalence	Ieee -2019
18.	A Simple Synthesis Process for Combinational QCA Circuits: QSynthesizer	Ieee -2019
19.	Test Pattern Generator for Majority Voter based QCA Combinational Circuits targeting MMC Defect	Ieee -2019
20.	Two Bit Overlap: A Class of Double Error Correction One Step Majority Logic Decodable Codes	Ieee -2019
21.	A Majority-Based Imprecise Multiplier for Ultra-Efficient Approximate Image Multiplication	Ieee -2019
22.	Design and Analysis of Majority Logic Based Approximate Adders and Multipliers	Ieee -2019
23.	A CMOS Majority Logic Gate and Its Application to One-Step ML Decodable Codes	Ieee -2019
24.	Novel Reliable QCA Subtractor Designs using Clock zone based Crossover	Ieee -2019
25.	Inversions Optimization in XOR-Majority Graphs with an Application to QCA	Ieee -2019
26.	Exact Synthesis of Boolean Functions in Majority-of-Five Forms	Ieee -2019
27.	New Majority Gate-Based Parallel BCD Adder Designs for Quantum-Dot Cellular Automata	Ieee -2019
28.	A Novel Iterative Reliability-Based Majority-Logic Decoder for NB-LDPC Codes	Ieee -2019
29.	Design and Simulation of 4-bit QCA BCD Full-adder	Ieee -2019
30.	An Efficient Design of 4 - to - 2 Encoder and Priority Encoder Based on 3-dot QCA Architecture	Ieee -2019

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31.	An Effective Design of 2 : 1 Multiplexer and 1 : 2 Demultiplexer using 3-dot QCA Architecture	Ieee -2019
32.	High Speed Memory Cell with Data Integrity in QCA	Ieee -2019
33.	Design of an Efficient Multilayer Arithmetic Logic Unit in Quantum-Dot Cellular Automata (QCA)	Ieee -2019
34.	Comparative Analysis of Full Adder Custom Design Circuit using Two Regular Structures in Quantum-Dot Cellular Automata (QCA)	Ieee -2019
35.	Design of efficient quantum Dot cellular automata (QCA) multiply accumulate (MAC) unit with power dissipation analysis	Ieee -2019
36.	QCA Realization of Reversible Gates Using Layered T Logic Reduction Technique	Ieee -2019
37.	QCA Based Error Detection Circuit for Nano Communication Network	Ieee -2019
38.	Hamming Code Generators using LTEx Module of Quantum-dot Cellular Automata	Ieee -2019
39.	A Design and Implementation of Montgomery Modular Multiplier	Ieee -2019
40.	Modified Binary Multiplier Circuit Based on Vedic Mathematics	Ieee -2019
41.	Performance Analysis of Wallace Tree Multiplier with Kogge Stone Adder using 15-4 Compressor	Ieee -2019
42.	Implementation of Floating Point Unit based on Booth Multiplier and Compressor Adder	Ieee -2019
43.	Digit-Serial Versatile Multiplier Based on a Novel Block Recombination of the Modified Overlap-Free Karatsuba Algorithm	Ieee -2019
44.	Novel Bit-Parallel and Digit-Serial Systolic Finite Field Multipliers Over GF(2m) Based on Reordered Normal Basis	Ieee -2019

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45.	Low-Power Approximate Unsigned Multipliers With Configurable Error Recovery	Ieee -2019
46.	Energy-efficient VLSI implementation of multipliers with double LSB operands	Ieee -2019
47.	Design and Analysis of Approximate Redundant Binary Multipliers	Ieee -2019
48.	Low-Power High-Accuracy Approximate Multiplier Using Approximate High-Order Compressors	Ieee -2019
49.	TOSAM: An Energy-Efficient Truncation- and Rounding-Based Scalable Approximate Multiplier	Ieee -2019
50.	Design Of Area Efficient And Low Power 4-Bit Multiplier Based On Full- swing GDI technique	Ieee -2019
51.	Low Space Complexity GF(2m) Multiplier for Trinomials Using n -Term Karatsuba Algorithm	Ieee -2019
52.	Rounding Technique Analysis for Power-Area & Energy Efficient Approximate Multiplier Design	Ieee -2019
53.	Design and Analysis of High Performance Multiplier Circuit	Ieee -2019
54.	Comparative Performance Analysis of Karatsuba Vedic Multiplier with Butterfly Unit	Ieee -2019
55.	A Low Power Binary Square rooter using Reversible Logic	Ieee -2019
56.	LDPC check node implementation using reversible logic	Ieee -2019
57.	Area Efficient VLSI Architecture for Reversible Radix-2 FFT Algorithm using Folding Technique and Reversible Gate	Ieee -2019
58.	Efficient designs of reversible latches with low quantum cost	Ieee -2019
59.	Structured decomposition for reversible Boolean functions	Ieee -2019
60.	Design and synthesis of improved reversible circuits using AIG- and MIG-based graph data structures	Ieee -2019

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61.	Design of Reversible Arithmetic Logic Unit with Built-In Testability	Ieee -2019
62.	Embedding Functions Into Reversible Circuits: A Probabilistic Approach to the Number of Lines	Ieee -2019
63.	Chaos-Based Bitwise Dynamical Pseudorandom Number Generator On FPGA	Ieee -2019
64.	A High Performance Full-Word Barrett Multiplier Designed for FPGAs with DSP Resources	Ieee -2019
65.	Design and Execution of Enhanced Carry Increment Adder using Han-Carlson and Kogge-Stone adder Technique : Han-Carlson and Kogge-Stone adder is used to increase speed of adder circuitry	Ieee -2019
66.	Design and Performance Comparison among Various types of Adder Topologies	Ieee -2019
67.	A New High-speed and Low area Efficient Pipelined 128-bit Adder Based on Modified Carry Look-ahead Merging with Han-Carlson Tree Method	Ieee -2019
68.	16 Bit Power Efficient Carry Select Adder	Ieee -2019
69.	Implementation of an XOR Based 16-bit Carry Select Adder for Area, Delay and Power Minimization	Ieee -2019
70.	Carry based approximate full adder for low power approximate computing	Ieee -2019
71.	Analysis of 1- bit full adder using different techniques in Cadence 45nm Technology	Ieee -2019
72.	Area Efficient Architecture for high speed wide data adders in Xilinx FPGAs	Ieee -2019
73.	Design of Delay Efficient Hybrid Adder for High Speed Applications	Ieee -2019
74.	Power-Delay-Product, Area and Threshold-Loss Analysis of CMOS Full Adder Circuits	Ieee -2019

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75.	Design and Performance Analysis of 32 Bit VLSI Hybrid adder	Ieee -2019
76.	Static Delay Variation Models for Ripple-Carry and Borrow-Save Adders	Ieee -2019
77.	SEDA - Single Exact Dual Approximate Adders for Approximate Processors	Ieee -2019
78.	A Novel Framework for Procedural Construction of Parallel Prefix Adders	Ieee -2019
79.	Design of Swing Dependent XOR-XNOR Gates based Hybrid Full Adder	Ieee -2019
80.	Formal Probabilistic Analysis of Low Latency Approximate Adders	Ieee -2019
81.	High Precision, High Performance FPGA Adders	Ieee -2019
82.	Concurrent Error Detectable Carry Select Adder with Easy Testability	Ieee -2019
83.	Design Methodology to Explore Hybrid Approximate Adders for Energy-Efficient Image and Video Processing Accelerators	Ieee -2019
84.	Design Of 3 Bit Adder Using 6 Transistors In Mentor Graphics	Ieee -2019
85.	A Theoretical Framework for Quality Estimation and Optimization of DSP Applications Using Low-Power Approximate Adders	Ieee -2019
86.	Hybrid Logical Effort for Hybrid Logic Style Full Adders in Multistage Structures	Ieee -2019
87.	Power-Efficient Approximate SAD Architecture with LOA Imprecise Adders	Ieee -2019
88.	Efficient Modular Adder Designs Based on Thermometer and One-Hot Coding	Ieee -2019
89.	Design of a Scalable Low-Power 1-bit Hybrid Full Adder for Fast Computation	Ieee -2019

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90.	Block-based Carry Speculative Approximate Adder for Energy-Efficient Applications	Ieee -2019
91.	FPGA Based Performance Comparison of Different Basic Adder Topologies with Parallel Processing Adder	Ieee -2019
92.	A novel design gate based low cost configurable R0 puf using reversible logic gates	Ieee -2019

	A Decoder for Short BCH Codes With High Decoding Efficiency and Low Power for Emerging Memories	2019	Front End
1.	Approximate Reverse Carry Propagate Adder for Energy-Efficient DSP Applications	2019	Front End
2.	Architecture Optimization and Performance Comparison of Nonce-Misuse-Resistant Authenticated Encryption Algorithms	2019	Front End
3.	TOSAM:AnEnergy-EfficientTruncation-andRounding-BasedScalableApproximate Multiplier	2019	Front End
4.	Design And Analysis Of Approximate Redundant Binary Multipliers.	2019	Front end
5.	Rounding Technique Analysis Of Power-Area & Energy Efficient Approximate Multiplier Design	2019	Front end
6.	A Combined Arithmetic-High-Level Synthesis Solution to Deploy Partial Carry-Save Radix-8 Booth Multipliers in Datapath.	2019	Front end

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7.	Low Power High Accuracy Approximate Multiplier Using Approximate High Order Compressors.	2019	Front end
8.	Efficient Modular Adder Designs Based on Thermometer & One-Hot Encoding	2019	Front End
9.	Error Detection And Correction In SRAM Emulated TCAMs	2019	Front end
10.	Efficient Design For Fixed Width Adder Tree	2019	Front end
11.	Area –Time Efficient Streaming Architecture For Architecture For FAST And BRIEF Detector	2019	Front end
12.	Hard Ware Efficient Post Processing Architecture For True Random Number Generators	2019	Front end
13.	A Two Speed Radix -4 Serial –Parallel Multiplier	2019	Front end
14.	Low power approximate unsigned multipliers with configurable error recovery	2019	Front end
15.	Energy Quality Scalable Adders Based On Non Zeroing Bit Truncation	2019	Front end
16.	Double MAC On A DSP Boosting The Performance Of Convolutional Neural Networks On FPGAS	2019	Front end
17.	A Low-Power Parallel Architecture for Linear Feedback Shift Registers	2019	Front end
18.	Ultra-low-voltage GDI-based hybrid full adder design for area and energy-efficient computing systems	2019	BACK End
19.	Design Of Area Efficient And Low Power 4-Bit Multiplier Based On Full-swing GDI technique	2019	BACK End
20.	Multistage Linear Feedback Shift Register Counters With Reduced Decoding Logic in 130-nm CMOS for Large-Scale Array Applications	2019	BACK End
21.	Low-Power Near-Threshold 10T SRAM Bit Cells With Enhanced Data-Independent Read Port Leakage for Array Augmentation in 32-nm CMOS	2019	BACK End

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22.	Column selection enabled 10 T SRAM utilizing shared diff VDD WRITE and dropped VDD read for FFT on real data.	2019	BACK End
23.	Cell-state-distribution –assisted threshold voltage detector for NAND flash memory	2019	BACK End
24.	Efficient VLSI Implementation of a Sequential Finite Field Multiplier Using Reordered Normal Basis in Domino Logic	2019	BACK End
25.	An Approach to LUT Based Multiplier for Short Word Length DSP Systems	2018	Frontend
26.	Novel High speed Vedic Multiplier proposal incorporating Adder based on Quaternary Signed Digit number system	2018	Frontend
27.	FPGA Implementation of an Improved Watchdog Timer for Safety-critical Applications	2018	Frontend
28.	Unbiased Rounding for HUB Floating-point Addition	2018	Frontend
29.	A Low-Power Yet High-Speed Configurable Adder for Approximate Computing	2018	Frontend
30.	A Low-Power High-Speed Accuracy-Controllable Approximate Multiplier Design	2018	Frontend
31.	The Design and Implementation of Multi – Precision Floating Point Arithmetic Unit Based on FPGA	2018	Frontend
32.	Extending 3-bit Burst Error-Correction Codes With Quadruple Adjacent Error Correction	2018	Frontend
33.	Efficient Modular Adders based on Reversible Circuits	2018	Frontend
34.	MAES: Modified Advanced Encryption Standard for Resource Constraint Environments	2018	Frontend
35.	Chip Design for Turbo Encoder Module for In-Vehicle System	2018	Frontend

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36.	Low-Power and Fast Full Adder by Exploring New XOR and XNOR Gates	2018	Backend
37.	Low Power 4×4 Bit Multiplier Design using Dadda Algorithm and Optimized Full Adder	2018	Backend

2020 IEEE PROJECTS

2020	Controller Architecture for Memory BIST Algorithms
2020	Regeneration of Test Patterns for BIST by Using Artificial Neural Networks
2020	Realization of Built-In Self Test(BIST) Enabled Memory(RAM) Using VHDL and Implementation in Spartan6 FPGA board
2020	Test Scheduling for Low Transition Reusable LFSR based BIST in 3-D Stacked ICs
2020	A Self-Timed Ring based TRNG with Feedback Structure for FPGA Implementation
2020	Chaotic Ring Oscillator Based True Random Number Generator Implementations in FPGA
2020	Chaotic True Random Number Generator for Secure Communication Applications
2020	Design and Synthesis of LFSR based Random Number Generator
2020	Design of LFSR Circuit based on High Performance XOR gate
2020	A High-Performance Symmetric Hybrid Form Design for High-Order FIR Filters

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2020	FPGA Implementation of Symmetric Systolic FIR Filter using Multi-channel Technique
2020	High Performance, Low Power Architecture of 5-stage FIR Filter using Modified Montgomery Multiplier
2020	Power efficient FIR filter Architecture using Distributed Arithmetic Algorithm
2020	Application of Vedic Multiplier: Design of a FIR Filter
2020	Design of FIR filter based on FPGA
2020	Realization of Power Efficient FIR Filters using Hybrid Accurate-Inaccurate Adder Architecture

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