VLSI IEEE 2020-21 – FRONT END and BACK END

1.	Design and analysis of High speed wallace tree multiplier using parallel prefix adders for VLSI circuit designs
2.	Implementation of optimized digital filter using sklansky adder and kogge stone adder
3.	Analysis of 8-bit Vedic Multiplier using high speed CLA Adder
4.	An Efficient Implementation of FIR Filter Using High Speed Adders For Signal Processing Applications
5.	Design of 8 bit and 16 bit Reversible ALU for Low Power Applications
6.	High speed and efficient ALU using modified booth multiplier
7.	Design of Area Optimized Arithmetic and Logical Unit for Microcontroller
8.	Modified High Speed 32-bit Vedic Multiplier Design and Implementation
9.	Application of Vedic Multiplier: Design of a FIR Filter
10.	Analysis of 32-Bit Multiply and Accumulate unit (MAC) using Vedic Multiplier
11.	Design and Evaluation of a FIR Filter Using Hybrid Adders and Vedic Multipliers
12.	High Performance, Low Power Architecture of 5-stage FIR Filter using Modified Montgomery Multiplier
13.	Controller Architecture for Memory BIST Algorithms
14.	Realization of Built-In Self-Test(BIST) Enabled Memory(RAM) Using Verilog and Implementation in Spartan6 FPGA board
15.	A High-Performance Symmetric Hybrid Form Design for High-Order FIR Filter
16.	FPGA Implementation of Symmetric Systolic FIR Filter using Multi-channel Technique
17.	Power efficient FIR filter Architecture using Distributed Arithmetic Algorithm
18.	Design of FIR filter based on FPGA

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VLSI IEEE 2020-21 – FRONT END and BACK END

19.	Power efficient FIR filter Architecture using Distributed Arithmetic Algorithm
20.	Design and Analysis of LFSR based Random Number generator
21.	VLSI implementation of Turbo coder for lte using Verilog
22.	A Self-Timed Ring based TRNG with Feedback Structure for FPGA Implementation
23.	Area Efficient and Low Power Multiplexer based Data Comparator for Median filter in Denoising Application
24.	Low Power SEC-DED Hamming Code Using Reversible Logic
25.	Design of Reversible Shift Registers Minimizing Number of Gates, Constant Inputs and Garbage Outputs
26.	Design and performance analysis of Subtractor using 2:1 multiplexer using multiple logic families
27.	Leakage Power Reduction in CMOS Logic Circuits Using Stack ONOFIC Technique adder
28.	Power Efficient Design of Adiabatic Approach for Low Power VLSI Circuits
29.	Review On LFSR For LOW Power BIST
30.	Designing of Multiplexer and De-Multiplexer using different Adiabatic Logic
31.	A Novel Area Efficient Parity Generator and Checker Circuits Design Using QCA
32.	Design of Multiplexer Using Actin Quantum Cellular Automata
33.	Design of a High-Performance 2-bit Magnitude Comparator Using Hybrid Logic Style
34.	Design and Implementation of Primitive Cells, Full Adder, Full Subtractor, and Multiplier using Modified Gate Diffusion Input Logic

VLSI IEEE 2020-21 – FRONT END and BACK END

35.	Realization of Power Efficient FIR Filters using Hybrid Accurate-Inaccurate Adder Architecture
36	Controller Architecture for Memory BIST Algorithms
37	Regeneration of Test Patterns for BIST by Using Artificial Neural Networks
38	Realization of Built-In Self Test(BIST) Enabled Memory(RAM) Using VHDL and Implementation in Spartan6 FPGA board
39	Test Scheduling for Low Transition Reusable LFSR based BIST in 3-D Stacked ICs
40	A Self-Timed Ring based TRNG with Feedback Structure for FPGA Implementation
41	Chaotic Ring Oscillator Based True Random Number Generator Implementations in FPGA
42	Chaotic True Random Number Generator for Secure Communication Applications
43	Design and Synthesis of LFSR based Random Number Generator
44	Design of LFSR Circuit based on High Performance XOR gate
45	A High-Performance Symmetric Hybrid Form Design for High-Order FIR Filters
46	FPGA Implementation of Symmetric Systolic FIR Filter using Multi-channel Technique
47	High Performance, Low Power Architecture of 5-stage FIR Filter using Modified Montgomery Multiplier
48	Power efficient FIR filter Architecture using Distributed Arithmetic Algorithm
49	Application of Vedic Multiplier: Design of a FIR Filter
50	Design of FIR filter based on FPGA
51	Realization of Power Efficient FIR Filters using Hybrid Accurate-Inaccurate Adder Architecture

2019 IEEE

1.	Approximate Reverse Carry Propagate Adder for Energy-Efficient DSP Applications	Front End
2.	Architecture Optimization and Performance Comparison of Nonce-Misuse-Resistant Authenticated Encryption Algorithms	Front End
3.	TOSAM:AnEnergy-EfficientTruncation-andRounding-BasedScalableApproximate Multiplier	Front End
4.	Design And Analysis Of Approximate Redundant Binary Multipliers.	Front end
5.	Rounding Technique Analysis Of Power-Area & Energy Efficient Approximate Multiplier Design	Front end

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VLSI IEEE 2020-21 – FRONT END and BACK END

6.	A Combined Arithmetic-High-Level Synthesis Solution to Deploy Partial Carry-Save Radix-8 Booth Multipliers in Datapath.	Front end
7.	Low Power High Accuracy Approximate Multiplier Using Approximate High Order Compressors.	Front end
8.	Efficient Modular Adder Designs Based on Thermometer & One-Hot Encoding	Front End
9.	Error Detection And Correction In SRAM Emulated TCAMs	Front end
10.	Efficient Design For Fixed Width Adder Tree	Front end
11.	Area –Time Efficient Streaming Architecture For Architecture For FAST And BRIEF Detector	Front end
12.	Hard Ware Efficient Post Processing Architecture For True Random Number Generators	Front end
13.	A Two Speed Radix -4 Serial –Parallel Multiplier	Front end
14.	Low power approximate unsigned multipliers with configurable error recovery	Front end
15.	Energy Quality Scalable Adders Based On Non Zeroing Bit Truncation	Front end
16.	Double MAC On A DSP Boosting The Performance Of Convolutional Neural Networks On FPGAS	Front end
17.	A Low-Power Parallel Architecture for Linear Feedback Shift Registers	Front end
18.	Ultra-low-voltage GDI-based hybrid full adder design for area and energy-efficient computing systems	BACK End
19.	Design Of Area Efficient And Low Power 4-Bit Multiplier Based On Full-swing GDI technique	BACK End
20.	Multistage Linear Feedback Shift Register Counters With Reduced Decoding Logic in 130-nm CMOS for Large-Scale Array Applications	BACK End
21.	Low-Power Near-Threshold 10T SRAM Bit Cells With Enhanced Data-Independent Read Port Leakage for Array Augmentation in 32-nm CMOS	BACK End
22.	Column selection enabled 10 T SRAM utilizing shared diff VDD WRITE and dropped VDD read for FFT on real data.	BACK End
23.	Cell-state-distribution –assisted threshold voltage detector for NAND flash memory	BACK End
24.	Efficient VLSI Implementation of a Sequential Finite Field Multiplier Using Reordered Normal Basis in Domino Logic	BACK End
25.	An Approach to LUT Based Multiplier for Short Word Length DSP Systems	Frontend

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VLSI IEEE 2020-21 – FRONT END and BACK END

26.	Novel High speed Vedic Multiplier proposal incorporating Adder based on Quaternary Signed Digit number system	Frontend
27.	FPGA Implementation of an Improved Watchdog Timer for Safety-critical Applications	Frontend
28.	Unbiased Rounding for HUB Floating-point Addition	Frontend
29.	A Low-Power Yet High-Speed Configurable Adder for Approximate Computing	Frontend
30.	A Low-Power High-Speed Accuracy-Controllable Approximate Multiplier Design	Frontend
31.	The Design and Implementation of Multi – Precision Floating Point Arithmetic Unit Based on FPGA	Frontend
32.	Extending 3-bit Burst Error-Correction Codes With Quadruple Adjacent Error Correction	Frontend
33.	Efficient Modular Adders based on Reversible Circuits	Frontend
34.	MAES: Modified Advanced Encryption Standard for Resource Constraint Environments	Frontend
35.	Chip Design for Turbo Encoder Module for In-Vehicle System	Frontend
36.	Low-Power and Fast Full Adder by Exploring New XOR and XNOR Gates	Backend

2018 IEEE

1.	First experimental demonstration of a scalable linear majority gate based on spin waves
2.	Design of Majority Logic Based Comparator
3.	Novel Cascadable Magnetic Majority Gates for Implementing Comprehensive Logic Functions
4.	Comparator Design using CTL and Outputwired based Majority Gate
5.	Design of Generalized Pipeline Cellular Array in Quantum-Dot Cellular Automata
6.	Size Optimization of MIGs with an Application to QCA and STMG Technologies
7.	Spin-based majority gates for logic applications
8.	Finite Hyperplane Codes: Minimum Distance and Majority-Logic Decoding
9.	Adapting Computer Arithmetic Structures to Sustainable Supercomputing in Low-Power, Majority-Logic Nanotechnologies
10.	A Novel Design of Quantum-Dots Cellular Automata Comparator Using Five-Input Majority Gate
11.	Modified majority logic decoding of Reed–Muller codes using factor graphs
12.	Characteristics of signal propagation in multiferroic majority logic gates subjected to thermal noise

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13.	Bit error probability analysis for majority logic decoding of CSOC codes over fading channels
14.	Majority Voting-Based Reduced Precision Redundancy Adders
15.	On the Decoding Radius Realized by Low-Complexity Decoded Non-Binary Irregular LDPC Codes
16.	Design of 2's Complement of 4-Bit Binary Numbers Using Quantum Dot Cellular Automata
17.	Majority Logic: Prime Implicants and n-Input Majority Term Equivalence
18.	A Simple Synthesis Process for Combinational QCA Circuits: QSynthesizer
19.	Test Pattern Generator for Majority Voter based QCA Combinational Circuits targeting MMC Defect
20.	Two Bit Overlap: A Class of Double Error Correction One Step Majority Logic Decodable Codes
21.	A Majority-Based Imprecise Multiplier for Ultra-Efficient Approximate Image Multiplication
22.	Design and Analysis of Majority Logic Based Approximate Adders and Multipliers
23.	A CMOS Majority Logic Gate and Its Application to One-Step ML Decodable Codes
24.	Novel Reliable QCA Subtractor Designs using Clock zone based Crossover
25.	Inversions Optimization in XOR-Majority Graphs with an Application to QCA
26.	Exact Synthesis of Boolean Functions in Majority-of-Five Forms
27.	New Majority Gate-Based Parallel BCD Adder Designs for Quantum-Dot Cellular Automata
28.	A Novel Iterative Reliability-Based Majority-Logic Decoder for NB-LDPC Codes
29.	Design and Simulation of 4-bit QCA BCD Full-adder
30.	An Efficient Design of 4 - to - 2 Encoder and Priority Encoder Based on 3-dot QCA Architecture
31.	An Effective Design of 2 : 1 Multiplexer and 1 : 2 Demultiplexer using 3-dot QCA Architecture
32.	High Speed Memory Cell with Data Integrity in QCA
33.	Design of an Efficient Multilayer Arithmetic Logic Unit in Quantum-Dot Cellular Automata (QCA)
34.	Comparative Analysis of Full Adder Custom Design Circuit using Two Regular Structures in Quantum-Dot Cellular Automata (QCA)
35.	Design of efficient quantum Dot cellular automata (QCA) multiply accumulate (MAC) unit with power dissipation analysis
36.	QCA Realization of Reversible Gates Using Layered T Logic Reduction Technique
37.	QCA Based Error Detection Circuit for Nano Communication Network
38.	Hamming Code Generators using LTEx Module of Quantum-dot Cellular Automata
39.	A Design and Implementation of Montgomery Modular Multiplier
40.	Modified Binary Multiplier Circuit Based on Vedic Mathematics
41.	Performance Analysis of Wallace Tree Multiplier with Kogge Stone Adder using 15-4 Compressor
42.	Implementation of Floating Point Unit based on Booth Multiplier and Compressor Adder

VLSI IEEE 2020-21 – FRONT END and BACK END

43.	Digit-Serial Versatile Multiplier Based on a Novel Block Recombination of the Modified Overlap-Free Karatsuba Algorithm
44.	Novel Bit-Parallel and Digit-Serial Systolic Finite Field Multipliers Over GF(2m) Based on Reordered Normal Basis
45.	Low-Power Approximate Unsigned Multipliers With Configurable Error Recovery
46.	Energy-efficient VLSI implementation of multipliers with double LSB operands
47.	Design and Analysis of Approximate Redundant Binary Multipliers
48.	Low-Power High-Accuracy Approximate Multiplier Using Approximate High-Order Compressors
49.	TOSAM: An Energy-Efficient Truncation- and Rounding-Based Scalable Approximate Multiplier
50.	Design Of Area Efficient And Low Power 4-Bit Multiplier Based On Full- swing GDI technique
51.	Low Space Complexity GF(2m) Multiplier for Trinomials Using n -Term Karatsuba Algorithm
52.	Rounding Technique Analysis for Power-Area & Energy Efficient Approximate Multiplier Design
53.	Design and Analysis of High Performance Multiplier Circuit
54.	Comparative Performance Analysis of Karatsuba Vedic Multiplier with Butterfly Unit
55.	A Low Power Binary Square rooter using Reversible Logic
56.	LDPC check node implementation using reversible logic
57.	Area Efficient VLSI Architecture for Reversible Radix-2 FFT Algorithm using Folding Technique and Reversible Gate
58.	Efficient designs of reversible latches with low quantum cost
59.	Structured decomposition for reversible Boolean functions
60.	Design and synthesis of improved reversible circuits using AIG- and MIG-based graph data structures
61.	Design of Reversible Arithmetic Logic Unit with Built-In Testability
62.	Embedding Functions Into Reversible Circuits: A Probabilistic Approach to the Number of Lines
63.	Chaos-Based Bitwise Dynamical Pseudorandom Number Generator On FPGA
64.	A High Performance Full-Word Barrett Multiplier Designed for FPGAs with DSP Resources
65.	Design and Execution of Enhanced Carry Increment Adder using Han-Carlson and Kogge-Stone adder Technique : Han-Carlson and Kogge-Stone adder is used to increase speed of adder circuitry
66.	Design and Performance Comparison among Various types of Adder Topologies
67.	A New High-speed and Low area Efficient Pipelined 128-bit Adder Based on Modified Carry Look-ahead Merging with Han-Carlson Tree Method
68.	16 Bit Power Efficient Carry Select Adder
69.	Implementation of an XOR Based 16-bit Carry Select Adder for Area, Delay and Power Minimization
70.	Carry based approximate full adder for low power approximate computing
71.	Analysis of 1- bit full adder using different techniques in Cadence 45nm Technology
72.	Area Efficient Architecture for high speed wide data adders in Xilinx FPGAs
73.	Design of Delay Efficient Hybrid Adder for High Speed Applications

74.	Power-Delay-Product, Area and Threshold-Loss Analysis of CMOS Full Adder Circuits
75.	Design and Performance Analysis of 32 Bit VLSI Hybrid adder
76.	Static Delay Variation Models for Ripple-Carry and Borrow-Save Adders
77.	SEDA - Single Exact Dual Approximate Adders for Approximate Processors
78.	A Novel Framework for Procedural Construction of Parallel Prefix Adders
79.	Design of Swing Dependent XOR-XNOR Gates based Hybrid Full Adder
80.	Formal Probabilistic Analysis of Low Latency Approximate Adders
81.	High Precision, High Performance FPGA Adders
82.	Concurrent Error Detectable Carry Select Adder with Easy Testability
83.	Design Methodology to Explore Hybrid Approximate Adders for Energy-Efficient Image and Video Processing Accelerators
84.	Design Of 3 Bit Adder Using 6 Transistors In Mentor Graphics
85.	A Theoretical Framework for Quality Estimation and Optimization of DSP Applications Using Low-Power Approximate Adders
86.	Hybrid Logical Effort for Hybrid Logic Style Full Adders in Multistage Structures
87.	Power-Efficient Approximate SAD Architecture with LOA Imprecise Adders
88.	Efficient Modular Adder Designs Based on Thermometer and One-Hot Coding
89.	Design of a Scalable Low-Power 1-bit Hybrid Full Adder for Fast Computation
90.	Block-based Carry Speculative Approximate Adder for Energy-Efficient Applications
91.	FPGA Based Performance Comparison of Different Basic Adder Topologies with Parallel Processing Adder
92.	A novel design gate based low cost configurable R0 puf using reversible logic gates